METHOD OF FORMING A SELF-ALIGNED CONTACT, AND METHOD OF FABRICATING A SEMICONDUCTOR DEVICE HAVING A SELF-ALIGNED CONTACT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of fabricating a semiconductor device. More particularly, the present invention relates to a technique of forming a self-aligned contact, and to a method of fabricating a semiconductor device having a self-aligned contact formed by such a technique.

2. Description of the Related Art

As semiconductor devices become smaller and smaller, the line width and the spacing between lines of the devices decrease. The resolution of a lithographic process used to form the lines of the semiconductor device must be increased to provide a smaller line width and spacing. However, the precision of an alignment technique, carried out to facilitate the lithographic process, can not be increased to comport with the increased resolution used to produce the fine line width and line spacing demanded of today's semiconductor devices. Accordingly, any misalignment during the fabrication of semiconductor must be minimized if a reduction in the size of semiconductor devices is to be achieved.

In the case of a semiconductor memory device, such as a dynamic random access memory (DRAM) including a capacitor, the capacitor is formed after a bit line is formed. A buried contact (BC) pad for electrically connecting the source/drain

region of a transistor to the storage electrode of the capacitor is formed after the bit line is formed. A long and deep contact hole, i.e., a contact hole having a high aspect ratio, is required to form the BC pad. However, it is not easy to secure an alignment margin sufficient for a lithographic process to produce a contact hole having a high enough aspect ratio. In particular, an alignment margin can not be secured for a design rule of 0.20 μm or smaller.

Recently, a technique of forming a self-aligned contact hole has been mainly used in connection with the forming of a BC pad. In this technique, a contact hole is formed by depositing an insulation layer on a lower conductive layer, and performing an etching process using the lower conductive layer and the insulation layer as a mask. This method will be described below with reference to FIGS. 1 - 5.

FIG. 1 shows the layout of a photoresist layer pattern used as an etching mask in the conventional method of forming a self-aligned contact. FIGS. 2 through 5 are sectional views taken along the line I-I′ of FIG. 1 and show the progression of the conventional method of forming a self-aligned contact.

In FIG. 1, reference numeral 100 denotes an active mask window for defining an active region and a field region. Reference numeral 110 denotes a gate mask window used for forming a gate stack pattern. Reference numeral 120 denotes a bit line mask window used for forming a bit line pattern. Reference numeral 130 denotes a photoresist layer pattern serving as an etching mask used for forming a self-aligned contact hole.

Referring to FIG. 2, isolation regions 210 defining active regions 205 are formed as trenches in a semiconductor substrate 200 using the active mask windows (100 in FIG. 1). A conductive film pad 220 is formed on each of the active region 205. A first interlayer insulation layer 230 is formed to completely cover the

conductive film pads 220. Next, bit line stacks 240 are formed on the first interlayer insulation layer 230 using the bit line mask windows (120 in FIG. 1). Each of the bit line stacks 240 is formed by sequentially forming a barrier metal layer 241, a bit line conductive layer 242 and a bit line capping layer 243 one upon the other. Subsequently, bit line spacers 250 are formed on the sidewalls of each of the bit line stacks 240.

Referring to FIG. 3, a second interlayer insulation layer 260 is formed to completely cover the bit line stacks 240 and the bit line spacers 250. Subsequently, the second interlayer insulation layer 260 is planarized such that the second interlayer insulation layer 260 has a predetermined thickness at the bit line stacks 250.

Referring to FIG. 4, a photoresist film pattern 130 is formed on the second interlayer insulation layer 260. The photoresist film pattern 130 is formed such that only those portions of the second interlayer insulation layer 260 between the bit line stacks 240 are exposed, and the remaining portions of the second interlayer insulation layer 260 are covered, as is also well shown in FIG. 1. After the photoresist film pattern 130 is formed, the second interlayer insulation layer 260 and the first interlayer insulation layer 230 are etched using the photoresist film pattern 130 as an etching mask. As a result, contact holes 270 exposing the top surfaces of the conductive film pads 220 are formed, as shown in FIG. 5. Conductive plugs (not shown) can be formed by filling the contact holes 270 with conductive material.

As the integration density of semiconductor devices increases, it becomes more difficult to etch the insulation layers to form the contact holes 270 due to the accumulation of polymer. Thus, the amount of polymer generated during the etching process must be somehow limited to prevent the etching process from stopping

prematurely. However, reducing the amount of polymer that will be generated is accompanied by a reduction in the selection ratio with respect to the bit line spacers 250 formed of silicon nitride. Therefore, when this countermeasure is taken, the bit line spacers 250 will be etched when the mask 130 is even slightly misaligned. When the bit line spacers 250 are over-etched, the bit line conductive layer 242 may be exposed, as shown at part A in FIG. 5. As a result, the conductive plug filling the contact hole will directly contact the bit line conductive layer 242, whereby the lower electrode of a capacitor and the bit line are short-circuited.

SUMMARY OF THE INVENTION

A first object of the present invention is to solve the above-described problems by providing a method of forming a self-aligned contact characterized by an alignment margin sufficient to prevent a short from being created between adjacent conductive layers.

To achieve this object, the present invention provides a method in which gate stacks are formed in a striped pattern on a semiconductor substrate, gate spacers are formed on the sidewalls of the gate stacks, conductive film pads serving as buried contact pads are formed between the gate spacers, a first interlayer insulation layer is formed on the conductive film pads and the gate stacks, bit line stacks are formed on the first interlayer insulation layer in a striped pattern extending crosswise relative to the striped pattern of the gate stacks, bit line spacers are formed on the sidewalls of the bit line stacks, a second interlayer insulation layer is formed on the first interlayer insulation layer in such a way that the upper surfaces of the bit line stacks are exposed, and a photoresist film pattern is formed on the second interlayer insulation layer in a striped pattern parallel to the striped pattern of

the gate stacks. The photoresist film pattern exposes segments of the bit line stacks and portions of the second interlayer insulation layer disposed directly above respective ones of the conductive film pads. Contact holes exposing the conductive film pads are formed by etching the second interlayer insulation layer and the first interlayer insulation layer using the photoresist film pattern, the bit line stacks and the bit line spacers as etching masks. The conductive plugs contacting the conductive film pads are formed by filling the contact holes with a conductive material.

Preferably, each of the gate stacks includes a gate insulation layer, a gate conductive layer and a gate capping layer which are sequentially formed one atop the other on the semiconductor substrate, and each of the bit line stacks includes a barrier metal layer, a bit line conductive layer and a bit line capping layer which are sequentially formed one atop the other on the first interlayer insulation layer.

The second interlayer insulation is preferably formed by covering the first interlayer insulation layer and the bit line stacks with a layer of insulating material, and completely planarizing the layer, i.e., until the upper surfaces of the bit line stacks are exposed. The planarization may be performed using chemical mechanical polishing.

The conductive plug is preferably formed by depositing enough conductive material to fill the contact holes and cover the bit line stacks, and planarizing the result to expose the upper surfaces of the bit line stacks. The planarization may be performed using an etch back technique or chemical mechanical polishing.

Another object of the present invention is to provide a semiconductor device that is also free of the above-described problems of the prior art.

To achieve this object, the technique of forming a self-aligned contact as summarized above is incorporated into an overall method of manufacturing a semiconductor device as follows. After the conductive plugs are formed, a third interlayer insulation layer, an etch stop layer, an oxide layer and a hard mask layer are sequentially formed on the conductive plugs, the bit line stacks and the second interlayer insulation layer. A second photoresist film pattern is then formed on the hard mask layer. The hard mask layer and the oxide layer are etched using the second photoresist film pattern as an etching mask, this etching terminating when the etch stop layer is reached (exposed). Next, the second photoresist film pattern is removed. Second contact holes for use in forming capacitor lower electrodes are themselves formed by sequentially removing the exposed portions of the etch stop layer and third interlayer insulation layer using the hard mask layer as an etching mask. In this way, the second contact holes expose the conductive plugs.

The second contact holes are filled with a conductive material to form capacitor lower electrodes contacting the conductive plugs.

Preferably, the etch stop layer is formed of a material having an etching selection ratio with respect to the oxide layer. In particular, the etching stop layer is preferably a silicon nitride layer. The third interlayer insulation layer is preferably formed of a material having an etching selection ratio with respect to the etch stop layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description of the

preferred embodiments thereof made with reference to the attached drawings, of which:

FIG. 1 is a plan view of a photoresist layer pattern used as an etching mask in performing an etching process in a conventional method of forming a self-aligned contact;

FIGS. 2 through 5 are sectional views of a lower portion of a semiconductor device, each taken along line I-I′ of FIG. 1, and together illustrating the progression of the conventional method of forming a self-aligned contact;

FIG. 6 is a plan view of a buried contact (BC) pad and a direct contact (DC) pad which are formed by a method of forming a self-aligned contact according to the present invention;

FIG. 7 is a plan view of a photoresist layer pattern used as an etching mask in performing an etching process in a method of forming a self-aligned contact according to the present invention;

FIGS. 8A, 9A, 10A and 11A are sectional views of a lower portion of a semiconductor device, each taken along line II-II′ of FIGS. 6 and 7 and together illustrating the progression of a method of forming a self-aligned contact according to the present invention;

FIGS. 8B, 9B, 10B and 11B are sectional views of a lower portion of a semiconductor device, each taken along line III-III′ of FIGS. 6 and 7 and together illustrating a method of forming a self-aligned contact according to the present invention;

FIGS. 12A, 13A and 14A are sectional views of a semiconductor device, each taken along line II-II′ of FIG. 7, and together illustrating a method of manufacturing a

semiconductor device having a self-aligned contact according to the present invention; and

FIGS. 12B, 13B and 14B are sectional views of a semiconductor device, each taken along line III-III′ of FIG. 7, and together illustrating a method of manufacturing a semiconductor device having a self-aligned contact according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Hereinafter, embodiments of the present invention will be described in detail with reference to the attached drawings. In the drawings, the size and shapes of elements are exaggerated for the sake of clarity, and the same reference numerals denote like elements throughout the drawings. Also, when a layer is described as being disposed on another layer or on a semiconductor substrate, such description means that the layer can be directly disposed directly the other layer or semiconductor substrate or that an interlayer(s) can be present therebetween.

Referring first to FIGS. 6 and/or 7, reference numeral 600 denotes an active mask window for defining an active region and a filed region. Reference numeral 610 denotes a gate mask window for forming a gate stack pattern. Reference numeral 620 denotes a bit line mask window for forming a bit line pattern. Reference numeral 630 denotes a photoresist film pattern as an etching mask for forming a self-aligned contact hole.

Referring to FIGS. 6, 7, 8A and 8B, isolation regions 710 defining active regions 705 are formed on a substrate 700 using the active masks 600. The isolation regions 710 are shown in the form of trenches, but may take other forms. For example, the isolation regions 710 may be formed using LOCal Oxidation of

Silicon (LOCOS). Next, gate stacks 610 are formed on the respective active regions 705 using the gate masks 610. Each of the gate stacks 610 may be formed by sequentially stacking and patterning a gate insulation layer 611, a gate conductive layer 612 and a gate capping layer 613. A metal silicide may be interposed between the gate conductive layer 612 and the gate capping layer 613 to reduce gate resistance. Next, gate spacers 615 are formed to cover the sidewalls of the gate stacks 610. The gate spacers 615 and the gate capping layers 613 are formed of silicon nitride having a selection ratio with respect to silicon oxide.

After the gate spacers 615 are formed, a typical lithographic method comprising exposure and development processes is performed to form a photoresist film pattern (not shown). Subsequently, an insulation layer (not shown) between the gate spacers 615 is etched using the photoresist film pattern as an etching mask, thereby forming contact holes exposing the surface of the semiconductor substrate 700 between the gate spacers 615. The contact holes are filled with a conductive material, for example, a polysilicon film, and an etch back process or a chemical mechanical planarization process is performed, thereby forming conductive film pads 720. Each of these conductive film pads 720 is used as a BC pad or a DC pad.

After the conductive film pads 720 are formed, a first interlayer insulation layer 730 is formed to cover the conductive film pads 720. Subsequently, bit line stacks 740 are formed on the first interlayer insulation layer 730 using the bit line mask windows 620 shown in FIG. 7. Each of the bit line stacks 740 may be formed by sequentially stacking a barrier metal layer 741, a bit line conductive layer 742 and a bit line capping layer 743 one on the other. Next, bit line spacers 750 are formed on the sidewalls of the bit line stacks 740 using a known method per se.

Referring to FIGS. 9A and 9B, a second interlayer insulation layer 760 is formed to completely cover the exposed surface of the first interlayer insulation layer 730, the bit line stacks 740 and the bit line spacers 750. Next, an etch back process or a chemical mechanical polishing process is performed to planarize the second interlayer insulation layer 760. When the chemical mechanical polishing is performed, the top surfaces of the bit line capping layers 743 are exposed at the completion of the process. Such a complete planarization is performed in order to minimize variations in the thickness of the second interlayer insulation layer 760 during subsequent processes.

Subsequently, a photoresist film is formed on the second interlayer insulation layer 760 and the bit line capping layers 743. The photoresist film is patterned to form a photoresist film pattern 630. As shown in FIG. 7, the gate stacks 610 are in the form of stripes, and the photoresist film pattern 630 comprises discrete laterally spaced apart stripes that directly overlie parts of the gate stacks 610 as extending parallel to the gate stacks 610. In other words, the photoresist film pattern 630 covers the insulation layers to one side only of each gate stack 610 and covers the conductive film pads 720 acting as DC pads, but exposes the insulation layers over the conductive film pads 720 acting as BC pads and the bit line stacks 740. Accordingly, the photoresist film pattern 630 is not shown in the sectional view of FIG. 9A that is taken along line II-II′ of FIG. 7 but is shown in the sectional view of FIG. 9B that is taken along line III-III′ of FIG. 7. By forming the photoresist film pattern 630 in a striped pattern, a sufficient alignment margin can be easily secured for the lithographic process for forming the photoresist film pattern.

Referring to FIGS. 10A and 10B, the second interlayer insulation layer 760 and the first interlayer insulation layer 730 are sequentially etched using the

photoresist film pattern 630 as an etching mask. During this etching process, the segments of the bit line stacks 740 that have already been exposed and the portions of the bit line spacers 750 that are exposed during the etching process act as an etching mask together with the photoresist film pattern 630. Because the photoresist film pattern 630 is in the form of stripes extending parallel to the gate stacks 610 and skewed (perpendicular) relative to the bit line stacks 740, the area of the underlying layer that is exposed is greater than that which is exposed using the conventional method. Thus, the etching process carried out when the present invention is practiced does not stop prematurely due to the presence of excessive polymer. Accordingly, an etching gas having a larger selection ratio with respect to the bit line capping layers 743 or the bit line spacers 750 can be used, to suppress the phenomenon in which the bit line capping layers 743 or the bit line spacers 750 are etched to the point where the bit line conductive layers 742 are exposed. After the etching process, contact holes 770 exposing the top surfaces of the conductive film pads 720 acting as BC pads are formed.

Referring to FIGS. 11A and 11B, conductive plugs 780 of polysilicon are formed within the contact holes 770. To this end, a polysilicon layer is formed on the entire surface of the resultant structure shown in FIGS. 10A and 10B. Then, an etch back process is performed to expose the surfaces of the bit line capping layers 743 of the bit line stacks 740. Consequently, the conductive plugs 780 are formed as isolated from one another other by the bit line stacks 740. Note, a chemical mechanical planarization process may be used instead of an etch back process.

A method of manufacturing a semiconductor device having a self-aligned contact according to the present invention will now be described with reference to FIGS. 7, and 12A - 14B.

First, referring to FIGS. 12A and 12B, conductive film pads 720, which are self-aligned contacts, and conductive plugs 780 are formed as was described with reference to FIGS. 8A through 11B. Next, a third interlayer insulation layer 790 is formed on the bit line stacks 740, second interlayer insulation layer 760 and conductive plugs 780. The third interlayer insulation layer 790 can be a silicon oxide layer. Subsequently, an etch stop layer 800 is formed on the third interlayer insulation layer 790. The etch stop layer 800 can be of silicon nitride like the bit line spacers 750. Silicon nitride and silicon oxide have etching selection ratios so that the bit line spacers 750 can be protected by the third interlayer insulation layer 790 during a subsequent process of removing the etch stopper 800. After the etch stop layer 800 is formed, a fourth interlayer insulation layer 810 is formed on the etch stop layer 800. For example, when the etch stop layer 800 is formed of a silicon nitride, the fourth interlayer insulation layer 810 is formed of a silicon oxide. Next, a hard mask layer 820 and an anti-reflection layer 830 are sequentially formed on the fourth interlayer insulation layer 810. A photoresist film pattern 840 is formed on the anti-reflection layer 830.

Referring to FIGS. 13A and 13B, the anti-reflection layer 830, the hard mask layer 820 and the fourth interlayer insulation layer 810 are sequentially etched using the photoresist film pattern 840 shown in FIGS. 12A and 12B as an etching mask, until the surface of the etch stopper 800 is partially exposed. As described above, the etching process is terminated once the surface of the etch stop layer 800 is exposed because the etch stop layer 800 and the fourth interlayer insulation layer 810 are formed of materials having large etching selection ratios. The photoresist film pattern 840 is removed after the etching process is completed.

Referring to FIGS. 14A and 14B, the exposed etch stop layer 800 and the anti-reflection layer 830 shown in FIGS. 13A and 13B are removed, thereby partially exposing the third interlayer insulation layer 790 and the hard mask layer 820. The exposed portions of the third interlayer insulation layer 790 are removed by etching using the hard mask layer 820 as an etching mask, thereby completing the contact holes 840 and thus, exposing the upper surfaces of the conductive plugs 780.

Subsequently, the contact holes 840 are filled with a conductive material, thereby forming capacitor lower electrodes connected to active regions 705 through the conductive film pads 720 and the conductive plugs 780.

As described above, a method of forming a self-aligned contact and a method of manufacturing a semiconductor device incorporating the same have the following advantages.

Firstly, concerning the photoresist pattern that serves as an etching mask for forming the contact holes in which the conductive plugs are formed, the photoresist film pattern comprises stripes extending parallel to gate stacks and skewed relative to the bit line stacks, whereby a sufficient alignment margin between the photoresist film pattern and the bit line stacks is secured. In addition, the area of an underlying layer that can be exposed is greater in comparison with a conventional method of forming a contact. Accordingly, a premature termination of the etching process, due to an accumulation of polymer in the contact hole as it is being formed, can be prevented. Consequently, an etching gas having a larger selection ratio with respect to bit line capping layers or bit line spacers can be used, to suppress a phenomenon in which the bit line capping layers or the bit line spacers are etched to the point where the bit line conductive layers are exposed.

Secondarily, variations in the thickness of the second interlayer insulation layer can be minimized during subsequent processes because the surface of a bit line stack is exposed by performing a complete planarization of the second interlayer insulation layer.

Thirdly, an etch back process, that is simpler and more economical than a chemical mechanical planarization process, may be used to planarize a conductive layer in forming the conductive plugs as isolated from one.

Fourthly, contact holes for forming capacitor lower electrodes may be easily formed after the conductive plugs are formed, by forming an insulation layer having a predetermined thickness on the resultant structure.

Although the present invention has been described above in connection with the preferred embodiments thereof, various changes to and modifications of the preferred embodiments will become readily apparent to those of ordinary skill in the art. All such changes and modifications are seen to be within the true spirit and scope of the present invention as defined by the appended claims.